Revision Guide for AMD Family 10h Processors

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Advanced Micro Devices

Revision History

Date	Revision	Description
September 2008	3.28	Added Conventions and updated MSR register usage and CPUID functions throughout; Added DR-B3 to Table 1, Table 2 and Table 9; Updated brand information in Overview, Table 1, Table 4, Table 5, Table 6, Table 7 and Table 10; Simplified MSRC001_0140 OS Visible Work-around MSR0 (OSVW_ID_Length) and removed Table 8: OSVW_ID_Length Per Processor Revision; Added Table 8: Cross Reference of Product Revision to OSVW ID; Renumbered tables appropriately; Added #322, #326, #328, #336-#339, #342, #351-#353, #355; Updated Description and Suggested Workaround in erratum #263 and #293; Updated Fix Planned in erratum #312 and updated Table 9 for erratum #312; Corrected Description, Potential Effect on System and Suggested Workaround in erratum #319; Updated Documentation Support section.
February 2008	3.16	Added AMD Phenom™ brand information in Table 1 and Table 10; Added Mixed Silicon Support section; Added Table 2; Supported Mixed Silicon Revision Configurations and Deleted Table 9: Cross Reference of Product Revision to OSVW_ID and renumbered tables accordingly; Added AM2r2 String Tables 6 and 7; Updated MSRC001_0140 OS Visible Work-around MSR0 (OSVW_ID_Length) and MSRC001_0141 OS Visible Work-around MSR1 (OSVW_Status) sections for Osvwld0; Added errata #293, #295, #297-#298, #295, #300-#302, #308-#309, #312, #315, and #319; Editorial update to Suggested Workaround in erratum #254; Updated Fix Planned in erratum #263 and updated entry in Table 9; Updated Documentation Support section.
September 2007	3.00	Initial public release.

Revision Guide for AMD Family 10h Processors

Overview

The purpose of the *Revision Guide for AMD Family 10h Processors* is to communicate updated product information to designers of computer systems and software developers. This revision guide includes information on the following products:

- Quad-Core AMD Opteron™ Processor
- Embedded AMD Opteron Processor
- AMD Phenom™ Triple-Core Processor
- AMD Phenom Quad-Core Processor

This guide consists of three major sections:

- **Processor Identification:** This section, starting on page 7, shows how to determine the processor revision, program and display the processor name string, and construct the processor name string.
- **Product Errata:** This section, starting on page 16, provides a detailed description of product errata, including potential effects on system operation and suggested workarounds. An erratum is defined as a deviation from the product's specification, and as such may cause the behavior of the processor to deviate from the published specifications.
- **Documentation Support:** This section, starting on page 64, provides a listing of available technical support resources.

Revision Guide Policy

Occasionally, AMD identifies product errata that cause the processor to deviate from published specifications. Descriptions of identified product errata are designed to assist system and software designers in using the processors described in this revision guide. This revision guide may be updated periodically.

Conventions

Numbering

- **Binary numbers.** Binary numbers are indicated by appending a “b” at the end, e.g., 0110b.
- **Decimal numbers.** Unless specified otherwise, all numbers are decimal. This rule does not apply to the register mnemonics; register mnemonics all utilize hexadecimal numbering.
- **Hexadecimal numbers.** Hexadecimal numbers are indicated by appending an “h” to the end, e.g., 45F8h.
- **Underscores in numbers.** Underscores are used to break up numbers to make them more readable. They do not imply any operation. e.g., 0110_1100b.
- **Undefined digit.** An undefined digit, in any radix, is notated as a lower case “x”.

Register References and Mnemonics

In order to define errata workarounds it is sometimes necessary to reference processor registers. References to registers in this document use a mnemonic notation consistent with that defined in the *BIOS and Kernel Developer’s Guide (BKDG) for AMD Family 10h Processors*, order# 31116. Each mnemonic is a concatenation of the register-space indicator and the offset of the register. The mnemonics for the various register spaces are as follows:

- IOXXX: x86-defined input and output address space registers; XXX specifies the byte address of the I/O register in hex (this may be 2 or 3 digits). This space includes the I/O-Space Configuration Address Register (IOCF8) and the I/O-Space Configuration Data Port (IOCFC) to access configuration registers.
- FYxXXX: PCI-defined configuration space; XXX specifies the byte address of the configuration register (this may be 2 or 3 digits) in hex; Y specifies the function number. For example, F3x40 specifies the register at function 3, address 40h. Each processor node includes five functions, 0 through 4.
- FYxXXX_xZZZZZ: Port access through the PCI-defined configuration space; XXX specifies the byte address of the data port configuration register (this may be 2 or 3 digits) in hex; Y specifies the function number; ZZZZZ specifies the port address (this may be 2 to 7 digits) in hex. For example, F2x9C_x1C specifies the port 1Ch register accessed using the data port register at function 2, address 9Ch. Refer to the *BIOS and Kernel Developer’s Guide (BKDG) for AMD Family 10h Processors*, order# 31116 for access properties.

- APICXXX: APIC memory-mapped registers; XXX is the byte address offset from the base address in hex (this may be 2 or 3 digits). The base address for this space is specified by the APIC Base Address Register (APIC_BAR) at MSR1B.
- CPUID FnXXXX_XXXX_RRR: processor capabilities information returned by the CPUID instruction where the CPUID function is XXXX_XXXX (in hex). When a register is specified by RRR, the reference is to the data returned in that register. For example, CPUID Fn8000_0001_EAX refers to the data in the EAX register after executing CPUID instruction function 8000_0001h.
- MSRXXXX_XXXX: model specific registers; XXXX_XXXX is the MSR number in hex. This space is accessed through x86-defined RDMSR and WRMSR instructions.

Many register references use the notation "[]" to identify a range of registers. For example, F2x[1,0][4C:40] is a shorthand notation for F2x40, F2x44, F2x48, F2x4C, F2x140, F2x144, F2x148, and F2x14C.

Processor Identification

This section shows how to determine the processor revision, program and display the processor name string, and construct the processor name string.

Revision Determination

Figure 1 shows the format of the value from CPUID Fn0000_0001_EAX.

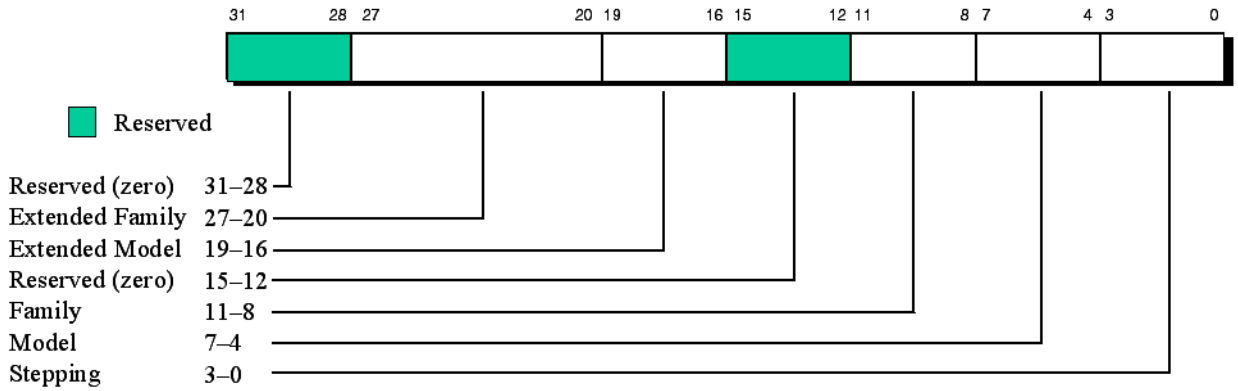

Figure 1. Format of CPUID Fn0000_0001_EAX

Table 1 shows the identification number from CPUID Fn0000_0001_EAX for each revision of the processor.

Table 1. CPUID Values for AMD Family 10h Processor Revisions

Revision	CPUID Fn0000_0001_EAX Value			
	Quad-Core AMD Opteron™ Processor	Embedded AMD Opteron™ Processor	AMD Phenom™ Triple-Core Processor	AMD Phenom™ Quad-Core Processor
DR-BA	00100F2Ah	00100F2Ah	N/Ah	N/Ah
DR-B2	00100F22h	00100F22h	00100F22h	00100F22h
DR-B3	00100F23h	00100F23h	00100F23h	00100F23h

Mixed Silicon Support

AMD Family 10h processors with different silicon revisions can be mixed in a multiprocessor system. Mixed silicon revision support includes the AMD Opteron™ processor configurations as shown in Table 2:

Table 2. Supported Mixed Silicon Revision Configurations

Silicon Revision	DR-BA	DR-B2	DR-B3
DR-BA	YES	YES	YES
DR-B2	YES	YES	YES
DR-B3	YES	YES	YES

Refer to Table 1 for CPUID values for these revisions. Errata workarounds must be applied according to revision as described in the Product Errata section starting on page 16 unless otherwise noted in the workraound of an erratum.

Programming and Displaying the Processor Name String

This section, intended for BIOS programmers, describes how to program and display the 48-character processor name string that is returned by CPUID Fn8000_000[4:2]. The hardware or cold reset value of the processor name string is 48 ASCII NUL characters, so the BIOS must program the processor name string before any general purpose application or operating system software uses the extended functions that read the name string. It is common practice for the BIOS to display the processor name string and model number whenever it displays processor information during boot up.

Note: *Motherboards that do not program the proper processor name string and model number will not pass AMD validation and will not be posted on the AMD Recommended Motherboard Web site.*

The name string must be ASCII NUL terminated and the 48-character maximum includes that NUL character.

The processor name string is programmed by MSR writes to the six MSR addresses covered by the range C001_00[35:30]h. Refer to the *BIOS and Kernel Developer's Guide (BKDG) for AMD Family 10h Processors*, order# 31116, for the format of how the 48-character processor name string maps to the 48 bytes contained in the six 64-bit registers of MSRC001_00[35:30].

The processor name string is read by CPUID reads to a range of CPUID functions covered by CPUID Fn8000_000[4:2]. Refer to CPUID Fn8000_000[4:2] in the *BIOS and Kernel Developer's Guide (BKDG) for AMD Family 10h Processors*, order# 31116, for the 48-character processor name string mapping to the 48 bytes contained in the twelve 32-bit registers of CPUID Fn8000_000[4:2].

Constructing the Processor Name String

This section describes how to construct the processor name string. BIOS uses the following fields to create the name string:

- BrandId[15:0] is from CPUID Fn8000_0001_EBX.
  - **String1[3:0]** is defined to be BrandID[14:11]. This field is an index to a string value used to create the processor name string. The definition of the String1 values are provided in Table 4 on page 10, and Table 6 on page 12.
  - **String2[3:0]** is defined to be BrandID[3:0]. This field is an index to a string value used to create the processor name string. The definition of the String2 values are provided in Table 5 on page 11, and Table 7 on page 12.
  - **Model[6:0]** is defined to be BrandID[10:4]. This field is used to create the model number in the name string. The model field represents a numerical model number which should be converted to ASCII for display of the model number.
  - **Pg[0]** is defined to be BrandID[15]. This field is used to index the appropriate page for the String1, String2, and Model values.

- PkgTyp[3:0] is from CPUID Fn8000_0001_EBX. This field specifies the package type as defined in the *BIOS and Kernel Developer's Guide (BKDG) for AMD Family 10h Processors*, order #31116, and is used to index the appropriate string tables from Table 3.
- NC[7:0] is from CPUID Fn8000_0008_ECX. This field identifies how many physical cores are present as defined in the *BIOS and Kernel Developer's Guide (BKDG) for AMD Family 10h Processors*, order #31116, and is used to index the appropriate strings from Table 4 on page 10, Table 5 on page 11, Table 6 on page 12, and Table 7 on page 12.

The name string is formed as follows:

1. Translate Model[6:0] into an ASCII value (*Model*), model numbers will range from 01-99. Model numbers less than 10 should include a leading zero, e.g., 09.
2. Select the appropriate string tables based on PkgTyp[3:0] from Table 3
3. Index into the referenced tables using String1[3:0], String2[3:0], and NC[7:0] to obtain the *String1* and *String2* values.
4. If *String1* is an undefined value skip step 5 and program the name string as follows:

   Name String = AMD Processor Model Unknown
5. Else concatenate the strings with the two character ASCII translation of Model[3:0] from step 1 to obtain the name string as follows:

   If *String2* is undefined, *Name string = String1, Model*

   Else, *Name string = String1, Model, String2*

Table 3. String Table Reference Per Package Type

PkgTyp [3:0]	String1 Table	String2 Table
0h	Table 4 on page 10	Table 5 on page 11
1h	Table 6 on page 12	Table 7 on page 12
2h-Fh	Reserved	Reserved

Table 4. String1 Values for Socket Fr2 (1207) Processors

Pg[0]	NC [7:0]	String1 [3:0]	Value	Note	Description
0b	03h	0h	`Quad-Core AMD Opteron(tm) Processor 83`	-	MP Server
		1h	`Quad-Core AMD Opteron(tm) Processor 23`	-	DP Server
1b	03h	1h	`Embedded AMD Opteron(tm) Processor`	1	Embedded
All other values			`AMD Processor Model Unknown`	-	

Table 5. String2 Values for Socket Fr2 (1207) Processors

Pg[0]	NC [7:0]	String2 [3:0]	Value	Note	Description
0b	03h	0Ah	SE	1	
		0Bh	HE	1	
	xxh	0Fh		2	
1b	03h	01h	GF HE	-	
		02h	HF HE	-	
All other values			Reserved	-	

Notes:

1. *The string includes a space as the leading character.*
2. *The String2 index 0Fh is defined as an empty string, i.e., no suffix.*

Table 6. String1 Values for Socket AM2r2 Processors

Pg[0]	NC [7:0]	String1 [3:0]	Value	Note	Description
0b	02h	0h	AMD Phenom(tm)	1	Client
0b	03h	0h	Quad-Core AMD Opteron(tm) Processor 13	-	UP Server
		2h	AMD Phenom(tm)	1	Client
All other values			AMD Processor Model Unknown	-	

Notes:

1. *The string includes a space as the trailing character.*

Table 7. String2 Values for Socket AM2r2 Processors

Pg[0]	NC [7:0]	String2 [3:0]	Value	Note	Description
0b	02h	0h	00 Triple-Core Processor	-	
		1h	00e Triple-Core Processor	-	
		2h	00B Triple-Core Processor	-	
		3h	50 Triple-Core Processor	-	
		4h	50e Triple-Core Processor	-	
		5h	50B Triple-Core Processor	-	
0b	03h	0h	00 Quad-Core Processor	-	
		1h	00e Quad-Core Processor	-	
		2h	00B Quad-Core Processor	-	
		3h	50 Quad-Core Processor	-	
		4h	50e Quad-Core Processor	-	
		5h	50B Quad-Core Processor	-	
All other values			Reserved	-	

F4x164 Fixed Errata Register

Communicating the status of an erratum requiring a workaround within a stepping of a processor family is necessary in certain circumstances. F4x164 is used to communicate the status of such an erratum fix so that BIOS or system software can determine the necessity of applying the workaround. Under these circumstances, the erratum workaround references the specified bit to enable software to test for the presence of the erratum. The revisions of a processor, prior to the definition of a bit may not be affected by the erratum. Therefore, software should use the stepping as the first criteria to identify the applicability of an erratum. Once defined, the definition of the status bit will persist within the family of processors.

Bits	Description
31:0	0000_0000h. Reserved.

MSRC001_0140 OS Visible Work-around MSR0 (OSVW_ID_Length)

This register, as defined in *AMD64 Architecture Programmer's Manual Volume 2: System Programming*, order# 24593, is used to specify the number of valid status bits within the OS Visible Work-around status registers.

The reset default value of this register is 0000_0000_0000_0000h.

BIOS shall program the OSVW_ID_Length to 0001h prior to hand-off to the OS.

Bits	Description
63:16	Reserved.
15:0	**OSVW_ID_Length: OS visible work-around ID length**. Read-write

MSRC001_0141 OS Visible Work-around MSR1 (OSVW_Status)

This register, as defined in *AMD64 Architecture Programmer's Manual Volume 2: System Programming*, order# 24593, provides the status of the known OS visible errata. Known errata are assigned an OSVW_ID corresponding to the bit position within the valid status field.

Operating system software should use MSRC001_0140 to determine the valid length of the bit status field. For all valid status bits: 1=Hardware contains the erratum, and an OS software work-around is required or may be applied instead of a BIOS workaround. 0=Hardware has corrected the erratum, so an OS software work-around is not necessary.

The reset default value of this register is 0000_0000_0000_0000h.

Bits	Description
63:1	**OsvwStatusBits:** Reserved. OS visible work-around status bits. Read-write.
0	**OsvwId0:** OsvwId0 1= Hardware contains erratum #298, an OS workaround may be applied if available. 0= Hardware has corrected erratum #298. In a multiprocessor platform, OsvwId0 should be set to 1 for all processors regardless of silicon revision when an affected processor is present. Read-write.

BIOS shall program the state of the valid status bits as shown in Table 8 prior to hand-off to the OS.

Table 8. Cross Reference of Product Revision to OSVW ID

Revision Number	MSRC001_1041 Bits
DR-BA	0000_0000_0000_0001h
DR-B2	0000_0000_0000_0001h
DR-B3	0000_0000_0000_0000h or 0000_0000_0000_0001h if mixed with DR-BA or DR-B2 processors in a multiprocessor platform

Product Errata

This section documents product errata for the processors. A unique tracking number for each erratum has been assigned within this document for user convenience in tracking the errata within specific revision levels. Table 9 cross-references the revisions of the part to each erratum. An "X" indicates that the erratum applies to the revision. The absence of an "X" indicates that the erratum does not apply to the revision. An "*" indicates advance information that the erratum has been fixed but not yet verified. "No fix planned" indicates that no fix is planned for current or future revisions of the processor.

Note: *There may be missing errata numbers. Errata that have been resolved from early revisions of the processor have been deleted, and errata that have been reconsidered may have been deleted or renumbered.*

Table 9. Cross-Reference of Product Revision to Errata

No.	Errata Description	Revision Number		
		DR-BA	DR-B2	DR-B3
57	Some Data Cache Tag Eviction Errors Are Reported As Snoop Errors	No fix planned		
60	Single Machine Check Error May Report Overflow	No fix planned		
77	Long Mode CALLF or JMPF May Fail To Signal GP When Callgate Descriptor is Beyond GDT/LDT Limit	No fix planned		
178	Default RdPtrInit Value Does Not Provide Sufficient Timing Margin	X	X	X
244	A DIV Instruction Followed Closely By Other Divide Instructions May Yield Incorrect Results	X	X	X
246	Breakpoint Due to An Instruction That Has an Interrupt Shadow May Be Delivered to the Hypervisor	X	X	X
248	INVLPGA of A Guest Page May Not Invalidate Splintered Pages	X		
254	Internal Resource Livelock Involving Cached TLB Reload	X	X	
260	REP MOVS Instruction May Corrupt Source Address	X	X	X
261	Processor May Stall Entering Stop-Grant Due to Pending Data Cache Scrub	No fix planned		
263	Incompatibility With Some DIMMs Due to DQS Duty Cycle Distortion	No fix planned		
264	Incorrect DRAM Data Masks Asserted When DRAM Controller Data Interleaving Is Enabled	X	X	X
269	ITT Specification Exceeded During Power-Up Sequencing	No fix planned		
273	Lane Select Function Is Not Available for Link BIST on 8-Bit HyperTransport™ Links In Ganged Mode	X	X	X
274	IDDIO Specification Exceeded During Power-Up Sequencing	X		
278	Incorrect Memory Controller Operation In Ganged Mode	X		
279	HyperTransport™ Link RTT and RON Specification Violations	X		
280	Time Stamp Counter May Yield An Incorrect Value	X	X	X
293	Memory Instability After PWROK Assertion	X	X	
295	DRAM Phy Configuration Access Failures		X	X
297	Single Machine Check Error May Report Overflow	No fix planned		
298	L2 Eviction May Occur During Processor Operation To Set Accessed or Dirty Bit	X	X	

Table 9. Cross-Reference of Product Revision to Errata (Continued)

No.	Errata Description	Revision Number		
		DR-BA	DR-B2	DR-B3
300	Hardware Memory Clear Is Not Supported After Software DRAM Initialization	X	X	X
301	Performance Counters Do Not Accurately Count MFENCE or SFENCE Instructions	X	X	X
302	MWAIT Power Savings May Not Be Realized when Two or More Cores Monitor the Same Address	X	X	X
308	Processor Stall in C1 Low Power State	X	X	X
309	Processor Core May Execute Incorrect Instructions on Concurrent L2 and Northbridge Response	X	X	
312	CVTSD2SS and CVTPD2PS Instructions May Not Round to Zero	X	X	X
315	FST and FSTP Instructions May Calculate Operand Address in Incorrect Mode	X	X	X
319	Inaccurate Temperature Measurement	X	X	X
322	Address and Command Fine Delay Values May Be Incorrect	No fix planned		
326	Misaligned Load Operation May Cause Processor Core Hang	X	X	X
328	BIST May Report Failures on Initial Powerup	X	X	X
336	Instruction Based Sampling May Be Inaccurate	X	X	X
337	CPU Instruction Based Sampling Fields May Be Inaccurate	X	X	X
338	Northbridge Instruction Based Sampling Fields May Be Inaccurate	X	X	X
339	APIC Timer Rollover May Be Delayed	No fix planned		
342	SMIs That Are Not Intercepted May Disable Interrupts	X	X	X
351	HyperTransport™ Technology LS2 Low-Power Mode May Not Function Correctly	X	X	X
352	SYSCALL Instruction May Execute Incorrectly Due to Breakpoint	No fix planned		
353	SYSRET Instruction May Execute Incorrectly Due to Breakpoint	No fix planned		
355	DRAM Read Errors May Occur at Memory Speeds Higher than DDR2-800	X	X	X

Table 10 cross-references the errata to each processor segment. An empty cell signifies that the erratum does not apply to the processor segment. “X” signifies that the erratum applies to the processor segment. “N/A” signifies that the erratum does not apply to the processor segment due to the silicon revision.

Table 10. Cross-Reference of Errata to Processor Segments

Errata Number	Quad-Core AMD Opteron™ Processor	Embedded AMD Opteron™ Processor	AMD Phenom™ Triple-Core Processor	AMD Phenom™ Quad-Core Processor
57	X	X	X	X
60	X	X	X	X
77	X	X	X	X
178	X	X	X	X
244	X	X	X	X
246	X	X	X	X
248	X	X	N/A	N/A
254	X	X	X	X
260	X	X	X	X
261	X	X	X	X
263	X	X	X	X
264	X	X	X	X
269	X	X	X	X
273	X	X	X	X
274	X	X	N/A	N/A
278	X	X	N/A	N/A
279	X	X	N/A	N/A
280	X	X	X	X
293	X	X	X	X
295	X	X	X	X
297	X	X	X	X
298	X	X	X	X
300	X	X	X	X
301	X	X	X	X
302	X	X	X	X
308	X	X	X	X
309	X	X	X	X
312	X	X	X	X
315	X	X	X	X
319	X	X	X	X
322	X	X	X	X
326	X	X		
328	X	X	X	X
336	X	X	X	X

Table 10. Cross-Reference of Errata to Processor Segments (Continued)

Errata Number	Quad-Core AMD Opteron™ Processor	Embedded AMD Opteron™ Processor	AMD Phenom™ Triple-Core Processor	AMD Phenom™ Quad-Core Processor
337	X	X	X	X
338	X	X	X	X
339	X	X	X	X
342	X	X	X	X
351	X	X	X	X
352	X	X	X	X
353	X	X	X	X
355			X	X

Table 11 cross-references the errata to each package type. An empty cell signifies that the erratum does not apply to the package type. “X” signifies that the erratum applies to the package type. “N/A” signifies that the erratum does not apply to the package type due to the silicon revision.

Table 11. Cross-Reference of Errata to Package Type

Errata Number	Socket Fr2 (1207)	Socket AM2r2
57	X	X
60	X	X
77	X	X
178	X	X
244	X	X
246	X	X
248	X	X
254	X	X
260	X	X
261	X	X
263	X	X
264	X	X
269	X	X
273	X	X
274	X	X
278	X	X
279	X	X
280	X	X
293	X	X
295	X	X
297	X	X
298	X	X
300	X	X
301	X	X
302	X	X
308	X	X
309	X	X
312	X	X
315	X	X
319	X	X
322	X	X
326	X	X
328	X	X
336	X	X
337	X	X
338	X	X

Table 11. Cross-Reference of Errata to Package Type (Continued)

Errata Number	Socket Fr2 (1207)	Socket AM2r2
339	X	X
342	X	X
351	X	X
352	X	X
353	X	X
355		X

57 Some Data Cache Tag Eviction Errors Are Reported As Snoop Errors

Description

In some cases, the machine check error code on a data cache (DC) tag array parity error erroneously classifies an eviction error as a snoop error.

The common cases of cache line replacements and external probes are classified correctly (as eviction and snoop respectively). The erroneous cases occur when a tag error is detected during a DC eviction that was generated by a hardware prefetch, a cache line state change operation, or a number of other internal microarchitectural events. In such cases, the error code logged in the DC Machine Check Status register (MC0_STATUS, MSR401) erroneously indicates a snoop error.

Potential Effect on System

Internally detected DC tag errors may be reported to software as having been detected by snoops. Depending upon machine check software architecture, the system response to such errors may be broader than necessary.

Suggested Workaround

None required.

Fix Planned

No

60 Single Machine Check Error May Report Overflow

Description

A single parity error encountered in the data cache tag array may incorrectly report the detection of multiple errors, as indicated by the overflow bit of the DC Machine Check Status register (bit 62 of MSR401).

Potential Effect on System

System software may be informed of a machine check overflow when only a single error was actually encountered.

Suggested Workaround

Do not rely on the state of the OVER bit in the DC Machine Check Status register.

Fix Planned

No

77 Long Mode CALLF or JMPF May Fail To Signal GP When Callgate Descriptor is Beyond GDT/LDT Limit

Description

If the target selector of a far call or far jump (CALLF or JMPF) instruction references a 16-byte long mode system descriptor where any of the last 8 bytes are beyond the GDT or LDT limit, the processor fails to report a General Protection fault.

Potential Effect on System

None expected, since the operating system typically aligns the GDT/LDT limit such that all descriptors are legal. However, in the case of erroneous operating system code, the above described GP fault will not be signaled, resulting in unpredictable system failure.

Suggested Workaround

None required, it is anticipated that long mode operating system code will ensure the GDT and LDT limits are set high enough to cover the larger (16-byte) long mode system descriptors.

Fix Planned

No

178 Default RdPtrInit Value Does Not Provide Sufficient Timing Margin

Description

Insufficient separation of the read pointer and write pointer in the synchronization FIFO can lead to setup violations in the transmit FIFO.

Potential Effect on System

The setup violations may lead to data corruption.

Suggested Workaround

BIOS should program F2x[1, 0]78[3:0] (RdPtrInit) to 5h.

Fix Planned

Yes

244 A DIV Instruction Followed Closely By Other Divide Instructions May Yield Incorrect Results

Description

A DIV instruction with a divisor less than 64 that is followed in close proximity by a DIV, IDIV, or AAM instruction may produce incorrect results.

Potential Effect on System

Possible data corruption.

Suggested Workaround

Contact your AMD representative for information on a BIOS update.

Fix Planned

Yes

246 Breakpoint Due to An Instruction That Has an Interrupt Shadow May Be Delivered to the Hypervisor

Description

A #DB exception occurring in guest mode may be delivered in the host context under the following conditions:

- A trap-type #DB exception is generated in guest mode during execution of an instruction with an interrupt shadow, and
- The instruction that generated the exception is immediately followed by an instruction resulting in #VMEXIT.

Potential Effect on System

Unpredictable results due to an unexpected #DB exception.

Suggested Workaround

The hypervisor should have a valid interrupt gate in the IDT of the #DB handler entry and the handler must be able to determine that this event has occurred. If the event is detected, the handler should execute an IRET back to the hypervisor; one method that could be used to evaluate for this condition is to compare the RIP pushed on the stack to the RIP of the instruction following VMRUN, if they are equivalent then this event has occurred.

Fix Planned

Yes

248 INVLPGA of A Guest Page May Not Invalidate Splintered Pages

Description

When an address mapped by a guest uses a larger page size than the host, the TLB entry created uses the size of the smaller page; this is referred to as page splintering. TLB entries that are the result of page splintering may not be invalidated when the large page is invalidated in the guest using INVLPGA.

Potential Effect on System

Unpredictable system behavior may result due to inconsistent entries in the TLB.

Suggested Workaround

The hypervisor should always intercept INVLPGA instructions. On returning to the guest from the INVLPGA intercept the hypervisor should set TLB_Control = 1 in the VMCB to ensure correctness.

Fix Planned

Yes

254 Internal Resource Livelock Involving Cached TLB Reload

Description

Under a highly specific and detailed set of conditions, an internal resource livelock may occur between a TLB reload and other cached operations.

Potential Effect on System

The system may hang.

Suggested Workaround

BIOS should set MSRC001_1023[21] to 1b.

Fix Planned

Yes

260 REP MOVS Instruction May Corrupt Source Address

Description

The processor may corrupt the source address for REP MOVS instructions using 16- or 32-bit addressing when a fault occurs on the first iteration and ECX is greater than 255 and EDI equals 0.

Potential Effect on System

Unpredictable system behavior.

Suggested Workaround

Contact your AMD representative for information on a BIOS update.

Fix Planned

Yes

261 Processor May Stall Entering Stop-Grant Due to Pending Data Cache Scrub

Description

The processor may stall if a correctable error is identified by the data cache scrubber within a small window of time before the processor enters a stop-grant state when another scrub is pending.

Potential Effect on System

The system may hang.

Suggested Workaround

BIOS should set MSRC001_1022[24].

Fix Planned

No

263 Incompatibility With Some DIMMs Due to DQS Duty Cycle Distortion

Description

Some DDR2 DIMMs exhibit a duty cycle distortion on the first DQS pulse of an incoming read request which may cause the processor's DRAM interface to miss a beat of data in a read burst.

Potential Effect on System

Undefined system behavior due to incorrect read data.

Suggested Workaround

If the memory is DDR2-533 or DDR2-667 write 00000800h to F2x[1, 0]9C_xD040F30, else write 00000000h to F2x[1, 0]9C_xD040F30.

The write of 00000000h to F2x[1, 0]9C_xD040F30 is not necessary if BIOS can not change the memory clock speed without a cold reset.

When exiting from the S4 or S5 state, apply this workaround prior to setting DRAM Configuration Low Register[InitDram] (F2x[1,0]90[0]). In addition, for DDR2-533 and DDR2-667, BIOS should set the DRAM read DQS timing control loop range to 32 during DQS position training.

When exiting from the S3 state, apply this workaround prior to setting DRAM Configuration Low Register[ExitSelfRef] (F2x[1,0]90[1]).

Fix Planned

No

264 Incorrect DRAM Data Masks Asserted When DRAM Controller Data Interleaving Is Enabled

Description

The processor may incorrectly assert the DRAM data masks for writes less than a cache line when DRAM controller data interleaving is enabled.

Potential Effect on System

Data corruption.

Suggested Workaround

BIOS should set MSRC001_001F[36] (DisDatMsk) to 1b when F2x110[5] (DctDatIntLv) is set to 1b.

Fix Planned

Yes

269 ITT Specification Exceeded During Power-Up Sequencing

Description

Processor current consumption may exceed the ITT maximum specified for C0/S0 operation if the VTT voltage regulator is enabled before the VDDIO voltage regulator and the VDDIO regulator enables a low resistance path to VSS while VTT - VDDIO > 400 mV.

Potential Effect on System

The VTT voltage regulator may shut down if ITT exceeds the platform design limit.

Suggested Workaround

None required if either of the following are true:

- The VTT regulator is enabled at the same time or after the VDDIO regulator.
- The VDDIO regulator does not enable a low resistance path to VSS while VTT - VDDIO > 400 mV.

For affected systems, the VTT voltage regulator should be enabled at the same time or after the VDDIO voltage regulator during power-up power sequencing. Existing specifications limiting the VDDIO to VTT relationship must be maintained.

Fix Planned

No

273 Lane Select Function Is Not Available for Link BIST on 8-Bit HyperTransport™ Links In Ganged Mode

Description

The link BIST engine incorrectly initiates tests on sublink 1 rather than sublink 0 under the following conditions:

- The HyperTransport™ link is configured as an 8-bit link in ganged mode,
- LaneSel[1], F0x[18C:170][13], is set to 1b,
- BistEn, F0x[18C:170][10], is set to 1b, and
- BIST is initiated by assertion of warm reset or a LDTSTOP_L disconnect.

Potential Effect on System

No impact to normal operational mode; however, the lane select function is not available for testing asymmetric links or isolation of errors to the uplink or downlink on symmetric links.

Suggested Workaround

None.

Fix Planned

Yes

274 IDDIO Specification Exceeded During Power-Up Sequencing

Description

Processor current consumption may exceed the IDDIO maximum specified for C0/S0 operation during power-up sequencing.

Potential Effect on System

None expected if the VDDIO voltage regulator is sourced by a RUN (running) plane from the power supply during power-up sequencing. Otherwise, during power-up sequencing the VDDIO voltage regulator may shut down if IDDIO exceeds the platform budget or the power supply may shut down if the SUS (suspend) rail current capacity is exceeded.

Suggested Workaround

Three options exist to ensure the VDDIO voltage regulator is sourced with sufficient current during processor power-up sequencing:

1. Enable the VDDIO voltage regulator after POWER_GOOD is asserted from the high-current (RUN) source rail.
2. Provide a path for a high-current (RUN) rail to source current to the VDDIO voltage regulator prior to POWER_GOOD assertion from the high-current (RUN) rail. This solution assumes the high-current (RUN) rail is enabled early enough relative to enabling the VDDIO voltage regulator.
3. Choose a power supply with increased capacity for the rail sourcing the VDDIO voltage regulator during power-up sequencing. The capacity required is system specific and should allocate 7 amps per processor in the power budget. The following is an example of a supply current capacity calculation assuming a 5 V suspend rail and 3 W rest of system power for a single-processor system. Other platform-specific factors such as power supply or regulator efficiencies should also be considered.
   - Rest of system (non-processor) power = 3 W
   - Processor power = 7 A/processor * 1 processor * 1.8 V = 12.6 W
   - Source rail capacity = (rest of system power + processor power) / source rail voltage; (3 W + 12.6 W) / 5 V = 3.12 A

Fix Planned

Yes

278 Incorrect Memory Controller Operation In Ganged Mode

Description

The DRAM controller 0 (DCT0) and DRAM controller 1 (DCT1) refresh counters may not be initialized to the same value using hardware controlled DRAM initialization when operating in ganged mode.

Potential Effect on System

Incorrect memory controller operation.

Suggested Workaround

BIOS should apply the following workaround prior to DRAM training when using hardware-controlled DRAM initialization and F2x110[4] (DctGangEn) is set to 1b.

1. Disable automatic refresh cycles by setting F2x8C[18] (DisAutoRefresh) to 1b.
2. Begin DRAM initialization by setting F2x90[0] to 1b.
3. Poll F2x90[0] until it reads 0b then wait at least 50 microseconds.
4. Enable automatic refresh cycles by clearing F2x8C[18] (DisAutoRefresh) to 0b.
5. Disable automatic refresh cycles by setting F2x8C[18] (DisAutoRefresh) to 1b.
6. Enable automatic refresh cycles by clearing F2x8C[18] (DisAutoRefresh) to 0b.
7. Begin DRAM training.

In addition, when resuming from S3, BIOS should apply the following workaround.

1. Disable automatic refresh cycles by setting F2x8C[18] (DisAutoRefresh) to 1b.
2. Initiate exit from self refresh by setting F2x90[1] to 1b.
3. Poll F2x90[1] until it reads 0b then wait at least 50 microseconds.
4. Enable automatic refresh cycles by clearing F2x8C[18] (DisAutoRefresh) to 0b.
5. Disable automatic refresh cycles by setting F2x8C[18] (DisAutoRefresh) to 1b.
6. Enable automatic refresh cycles by clearing F2x8C[18] (DisAutoRefresh) to 0b.

Fix Planned

Yes

279 HyperTransport™ Link R_{TT} and R_{ON} Specification Violations

Description

The R_{TT} and R_{ON} specifications for the HyperTransport™ link may be violated on some processor revisions.

Potential Effect on System

These violations do not result in any other HyperTransport™ link electrical specification violations. There are no known functional failures related to this problem.

Suggested Workaround

None required.

Fix Planned

Yes

280 Time Stamp Counter May Yield An Incorrect Value

Description

Reads of the time stamp counter may yield an inconsistent result.

Potential Effect on System

Undefined behavior for software that relies on a continuously increasing time stamp counter value.

Suggested Workaround

Contact your AMD representative for information on a BIOS upgrade.

Fix Planned

Yes

293 Memory Instability After PWROK Assertion

Description

The DRAM DQS DLL may not lock properly after PWROK is asserted.

Potential Effect on System

The system may have degraded memory margins leading to unreliable DRAM signaling. In some circumstances, this may cause BIOS to degrade the memory speed.

Suggested Workaround

During DRAM controller (DCT) initialization, system software should perform the following workaround to every DCT in the system:

1. Perform a dummy DRAM read to any address on any DIMM attached to the DCT.
2. Write 0000_8000h to register F2x[1, 0]9C_xD080F0C.
3. Wait at least 300 nanoseconds.
4. Write 0000_0000h to register F2x[1, 0]9C_xD080F0C.
5. Wait at least 2 microseconds.

When exiting from the S4 or S5 state, apply the workaround immediately prior to the Receiver Enable Training. During resume from the S3 state, apply the workaround after F2x[1, 0]90[ExitSelfRef] has been cleared and prior to restoring the F2x[1, 0]9C registers.

Fix Planned

Yes

295 DRAM Phy Configuration Access Failures

Description

Under a highly specific set of asynchronous timing conditions established during cold boot (S5 to S0 transition) or resume (S4 or S3 to S0 transition), the skew between the DRAM controllers (DCTs) and DRAM phy may lead to unreliable communication for DRAM phy configuration accesses.

Potential Effect on System

The system may hang during DRAM configuration accesses when using DCT link ganged mode ([DRAM Controller Select Low Register] F2x110[DctGangEn] = 1b), or fail DRAM training in link ganged mode or in link unganged mode.

Suggested Workaround

Contact your AMD representative for information on a BIOS update.

Fix Planned

Yes

297 Single Machine Check Error May Report Overflow

Description

A single tag snoop parity error encountered in the instruction cache tag array may incorrectly report the detection of multiple errors, as indicated by the overflow bit of the IC Machine Check Status register (MSR405[62]).

Potential Effect on System

System software may be informed of a machine check overflow when only a single error was actually encountered.

Suggested Workaround

None required.

Fix Planned

No

298 L2 Eviction May Occur During Processor Operation To Set Accessed or Dirty Bit

Description

The processor operation to change the accessed or dirty bits of a page translation table entry in the L2 from 0b to 1b may not be atomic. A small window of time exists where other cached operations may cause the stale page translation table entry to be installed in the L3 before the modified copy is returned to the L2.

In addition, if a probe for this cache line occurs during this window of time, the processor may not set the accessed or dirty bit and may corrupt data for an unrelated cached operation.

Potential Effect on System

One or more of the following events may occur:

- Machine check for an L3 protocol error. The MC4 status register (MSR410) will be equal to B2000000_000B0C0Fh or BA000000_000B0C0Fh. The MC4 address register (MSR412) will be equal to 26h.
- Loss of coherency on a cache line containing a page translation table entry.
- Data corruption.

Suggested Workaround

BIOS should set MSRC001_0015[3] (HWCR[TlbCacheDis]) to 1b and MSRC001_1023[1] to 1b.

In a multiprocessor platform, the workaround above should be applied to all processors regardless of silicon revision when an affected processor is present.

Fix Planned

Yes

300 Hardware Memory Clear Is Not Supported After Software DRAM Initialization

Description

When using software-controlled DRAM device initialization through EnDramInit (F2x[1, 0]7C DRAM Initialization Register[31]), hardware memory clear using MemClrInit (F2x110 DRAM Controller Select Low Register[3]) does not function.

Potential Effect on System

After BIOS sets MemClrInit (F2x110[3]), the hardware will not clear memory and will not set MemCleared (F2x110[10]). The BIOS will hang waiting for the operation to complete.

Suggested Workaround

BIOS should use hardware initialization of DRAM using InitDram (F2x[1, 0]90 DRAM Configuration Low Register[0]). If BIOS uses software initialization, alternative methods to initialize ECC must be used.

Fix Planned

Yes

301 Performance Counters Do Not Accurately Count MFENCE or SFENCE Instructions

Description

MFENCE and SFENCE instructions are not accurately counted by the performance monitor when MSRC001_000[3:0][7:0] (EventSelect) is 1D4h, or 1D5h.

Potential Effect on System

Performance monitoring software will not be able to count MFENCE and SFENCE instructions.

Suggested Workaround

None.

Fix Planned

Yes

302 MWAIT Power Savings May Not Be Realized when Two or More Cores Monitor the Same Address

Description

Execution of the MONITOR instruction may cause another core to exit the monitor event pending state.

Potential Effect on System

No functional impact; however, the power savings associated with the MWAIT instruction may not be realized.

Suggested Workaround

Contact your AMD representative for information on a BIOS update.

Fix Planned

Yes

308 Processor Stall in C1 Low Power State

Description

Under a highly specific set of internal timing conditions, an L3 eviction may stall for a processor core that has entered the C1 (Halt) state. If the processor core has already entered the low power state and the CpuPrbEn bit in the C1 SMAF is 0b (F3x84[24]), the stall persists until the processor core comes out of the low power state.

Potential Effect on System

The system may hang.

Suggested Workaround

Contact your AMD representative for information on a BIOS update.

Fix Planned

Yes

309 Processor Core May Execute Incorrect Instructions on Concurrent L2 and Northbridge Response

Description

Under a specific set of internal timing conditions, an instruction fetch may receive responses from the L2 and the Northbridge concurrently. When this occurs, the processor core may execute incorrect instructions.

Potential Effect on System

Unpredictable system behavior.

Suggested Workaround

BIOS should set MSRC001_1023[23].

Fix Planned

Yes

312 CVTSD2SS and CVTPD2PS Instructions May Not Round to Zero

Description

The Convert Scalar Double-Precision Floating Point to Scalar Single-Precision Floating Point (CVTSD2SS) and Convert Packed Double-Precision Floating Point to Packed Single-Precision Floating Point (CVTPD2PS) instructions do not round to zero when the Flush to Zero and Underflow Mask bits (MXCSR bits 15 and 11) are set to 1b and the double-precision operand is less than the smallest single-precision normal number.

Potential Effect on System

The conversion result will yield the smallest single-precision normalized number rather than zero. It is not expected that this will result in any anomalous software behavior since enabling flush to zero provides less precise results.

Suggested Workaround

None.

Fix Planned

Yes

315 FST and FSTP Instructions May Calculate Operand Address in Incorrect Mode

Description

A Floating-Point Store Stack Top (FST or FSTP) instruction in 64-bit mode that is followed shortly by an instruction that changes to compatibility mode may incorrectly calculate the operand address using compatibility mode. Also, an FST or FSTP instruction in compatibility mode that is followed shortly by an instruction that changes to 64-bit mode may incorrectly calculate the operand address using 64-bit mode.

The incorrect mode for address calculation is only used under highly specific internal timing conditions and when the Underflow Mask bit (FCW bit 4) is set and the data to be stored by the FST or FSTP instruction is a denormalized (tiny) number.

Potential Effect on System

The processor may store to an incorrect address. This may cause an unexpected page fault or unpredictable system behavior. This sequence has not been observed in any production software.

Suggested Workaround

Contact your AMD representative for information on a BIOS update.

Fix Planned

Yes

319 Inaccurate Temperature Measurement

Description

The internal thermal sensor used for CurTmp (F3xA4[31:21]), hardware thermal control (HTC), software thermal control (STC) thermal zone, and the sideband temperature sensor interface (SB-TSI) may report inconsistent values.

Potential Effect on System

HTC, STC thermal zone, and SB-TSI do not provide reliable thermal protection. This does not affect THERMTRIP or the use of the STC-active state through StcPstateLimit or StcPstateEn (F3x68[30:28, 5]).

Suggested Workaround

None. Systems should be designed with conventional thermal control and throttling methods or utilize PROCHOT_L functionality based on temperature measurements from an analog thermal diode (THERMDA/THERMDC).

Systems should not rely on the HTC features, STC thermal zone features, or use SB-TSI.

Software should not modify HtcTmpLmt (F3x64[22:16]) or enable any of the STC thermal zone features by setting StcApcTmpLoEn, StcApcTmpHiEn, StcSbcTmpLoEn, or StcSpcTmpHiEn (F3x68[3:0]).

Fix Planned

Yes

322 Address and Command Fine Delay Values May Be Incorrect

Description

The DRAM phy uses the memory speed at the time of DRAM initialization or self-refresh exit to adjust the fine delay values based on internal DLL settings. Data written to fine delay registers prior to DRAM initialization or self-refresh exit may be adjusted incorrectly.

No effect is observed for all fine delays except those in the DRAM Address/Command Timing Control Register at F2x[1,0]9C_x04; these are written after DRAM initialization. However, F2x[1,0]9C_x04 may be written before DRAM initialization or self-refresh exit and may result in an incorrect adjustment.

This erratum only affects MEMCLK frequencies of 400 MHz and higher.

Potential Effect on System

The system may have degraded memory margins leading to unreliable DRAM signaling.

Suggested Workaround

The following workaround should be applied by BIOS prior to writing F2x[1,0]9C_x04 during DRAM controller (DCT) initialization and during the S3 resume sequence:

1. Write 00000000h to F2x[1,0]9C_xD08E000.
2. In unganged mode (DRAM Controller Select Low Register [DctGangEn] (F2x110[4]) = 0b), if DRAM Configuration Register[MemClkFreq] (F2x[1,0]94[2:0]) is greater than or equal to 011b, write 00000080h to F2x[1,0]9C_xD02E001, else write 00000090h to F2x[1,0]9C_xD02E001.
3. In ganged mode (DRAM Controller Select Low Register [DctGangEn] (F2x110[4]) = 1b), if DRAM Configuration Register[MemClkFreq] (F2x94[2:0]) is greater than or equal to 011b, write 00000080h to F2x9C_xD02E001 and F2x19C_xD02E001, else write 00000090h to F2x9C_xD02E001 and F2x19C_xD02E001.

The write of 00000090h to F2x[1,0]9C_xD02E001 is not necessary if BIOS can not change the memory clock speed without a cold reset.

Fix Planned

No

326 Misaligned Load Operation May Cause Processor Core Hang

Description

Under a highly specific set of internal timing conditions, load operations with a misaligned operand may hang.

Any instruction loading data from memory without a LOCK prefix where the first byte and the last byte are in separate octal words may cause the condition mentioned above.

Potential Effect on System

Processor core hang.

Suggested Workaround

BIOS should clear MSRC001_1022[43:42].

Fix Planned

Yes

328 BIST May Report Failures on Initial Powerup

Description

When BIST is run after initial powerup, a non-zero (i.e., failing) value may be erroneously reported in EAX.

Subsequent BIST runs (induced by warm resets) are not affected by this erratum, and accurately report pass/fail as determined by the presence or absence of detectable defects in the structures tested.

Potential Effect on System

The processor may incorrectly represent itself as being defective on initial powerup. The system response to this is system software dependent.

Suggested Workaround

On initial powerup, system software should disregard the BIST result in EAX.

Fix Planned

Yes

336 Instruction Based Sampling May Be Inaccurate

Description

The processor may experience sampling inaccuracies when instruction based sampling (IBS) is enabled in the following cases:

- The IBS may not tag an operation when the current counter in IBS Execution Control Register[IbsOpCurCnt] (MSRC001_1033[51:32]) reaches the value in IBS Fetch Control Register[IbsOpMaxCnt] (MSRC001_1030[15:0], resulting in a missed sample. When this occurs, the IBS counter rolls over without an interrupt.
- The selection of instructions for IBS may be significantly skewed due to effects of instruction cache misses and branch prediction. As a result, certain instructions may be tagged less frequently than other instructions even when executed in the same code block.

Potential Effect on System

Inaccuracies in performance monitoring software may be experienced. Despite this erratum, IBS can be used effectively for identifying performance issues associated with specific instructions. The sampling bias makes IBS less effective for measuring statistical distribution of operations and events across a large code sequence on affected silicon revisions.

Suggested Workaround

None.

Fix Planned

Yes

337 CPU Instruction Based Sampling Fields May Be Inaccurate

Description

The processor may experience sampling inaccuracies when instruction based sampling (IBS) is enabled in the following fields:

- IBS Op Data Register[IbsCompToRetCtr] (MSRC001_1035[15:0]) may be incorrect for floating point instructions, when IBS Op Data 3 Register[IbsStOp] (MSRC001_1037[1]) is set, or when IBS Op Data 3 Register[IbsLdOp] (MSRC001_1037[0]) is set.
- IBS Op Data 3 Register[IbsDcMissLat] (MSRC001_1037[47:32]) may be incorrect if the processor tags a load instruction for IBS and the data for a retired store operation is in the process of being written to the data cache. As a result, IbsDcMissLat may start counting early when the load instruction is tagged and may be non-zero on a data cache hit.
- IBS Op Data 3 Register[IbsDcStToLdFwd, IbsDcL2TlbHit2M, IbsDcL2TlbMiss] (MSR_C001_1037[11, 6, 3]) may be incorrect when IBS Op Data 3 Register[IbsDcStBnkCon] (bit 10) or IBS Op Data 3 Register[IbsDcLdBnkCon] (bit 9) are set.
- IBS Op Data 3 Register[IbsLdOp, IbsStOp] (MSRC001_1037[1:0]) may be set incorrectly for non load/store instructions that are tagged for IBS. Other fields in MSRC001_1037 may also be set based on an unrelated instruction. This occurs when a load/store instruction is tagged and then a branch misprediction causes it to be canceled. When a new instruction is tagged for IBS, it may trigger incorrect information if the same buffers are used for both instructions. This typically would not result in a statistically significant number of incorrect samples.

Potential Effect on System

Inaccuracies in performance monitoring software may be experienced.

Suggested Workaround

None.

Fix Planned

Yes

338 Northbridge Instruction Based Sampling Fields May Be Inaccurate

Description

The IBS Op Data 2 Register[NbIbsReqDstProc] (MSRC001_1036[4]) may be incorrect when the Northbridge is performing back-to-back operations while an instruction tagged for instruction based sampling (IBS) is executed and IBS Op Data 2 Register[NbIbsReqSrc] (MSRC001_1036[2:0]) is 011b or 111b. This typically would not result in a statistically significant number of incorrect samples.

Potential Effect on System

Inaccuracies in performance monitoring software may be experienced.

Suggested Workaround

None.

Fix Planned

Yes

339 APIC Timer Rollover May Be Delayed

Description

The APIC timer does not immediately rollover when it transitions to zero and Timer Local Vector Table Entry[Mode] (APIC320[17]) is configured to run in periodic mode. In addition, when Timer Local Vector Table Entry[Mask] (APIC320[16]) is configured to generate an interrupt, the interrupt is also delayed whether configured for periodic or one-shot mode.

The per rollover error that may be observed is between 35 and 90 ns.

For systems that support C1E, the per rollover error may be as high as 640 ns if the roll over occurs while the processor is in the C1E state.

Potential Effect on System

None expected. The standard use of the APIC timer and the level of accuracy required does not make the error significant.

Suggested Workaround

None required.

Fix Planned

No

342 SMIs That Are Not Intercepted May Disable Interrupts

Description

During a resume from SMM that is due to an unintercepted SMI from a SVM guest context, the processor core does not restore the correct effective interrupt flag (IF) if the guest VMCB V_INTR_MASKING bit (offset 060h bit 24) is 1b. Under these circumstances, the effective interrupt flag may be zero.

SMIs are not intercepted if VMCB offset 00Ch bit 2 is 0b or HWCR[SmmLock] (MSRC001_0015[0]) is 1b.

Potential Effect on System

The guest context may run with interrupts disabled until the next guest intercept. The hypervisor may not be able to regain control and the system may hang.

Suggested Workaround

Contact your AMD representative for information on a BIOS update.

Fix Planned

Yes

351 HyperTransport™ Technology LS2 Low-Power Mode May Not Function Correctly

Description

The HyperTransport™ technology LS2 low-power state may not function correctly in all systems.

Potential Effect on System

System hang or video distortion due to excessive latency.

Suggested Workaround

System software should program the Link Extended Control Registers[LS2En] (F0x[18C:170][8]) to 0b for all links. This allows the LS1 low-power state to be used as an alternative to LS2.

Fix Planned

Yes

352 SYSCALL Instruction May Execute Incorrectly Due to Breakpoint

Description

A SYSCALL instruction will execute incorrectly and an incorrect debug exception will be taken when all of the following conditions are satisfied:

- An enabled instruction breakpoint address matches the RIP of the SYSCALL instruction.
- The processor is in 64-bit mode or compatibility mode.
- The instruction would not generate any other exception.
- SYSCALL Flag Mask Register[16] (MSRC000_0084[16]) is set to 1b.
- RFLAGS.RF is set to 1b.

Potential Effect on System

None expected during normal operation. Kernel debuggers may observe unpredictable system behavior.

Suggested Workaround

Operating system software should clear SYSCALL Flag Mask Register[16] (MSRC000_0084[16]) to 0b during initialization.

Fix Planned

Yes

353 SYSRET Instruction May Execute Incorrectly Due to Breakpoint

Description

A SYSRET instruction will execute incorrectly and an incorrect debug exception will be taken when all of the following conditions are satisfied:

- An enabled instruction breakpoint address matches the RIP of the SYSRET instruction.
- The processor is in 64-bit mode or compatibility mode.
- The instruction would not generate any other exception.
- R11[16] is cleared to 0b.
- RFLAGS.RF is set to 1b.

Potential Effect on System

None expected during normal operation. Kernel debuggers may observe unpredictable system behavior.

Suggested Workaround

Software should set R11[16] to 1b before executing the SYSRET instruction in 64-bit mode.

Fix Planned

Yes

355 DRAM Read Errors May Occur at Memory Speeds Higher than DDR2-800

Description

The processor DRAM interface may miss a beat of data under conditions of back-to-back read bursts to the same chip select using DDR2-1066 memory speed, resulting in incorrect data read by the DRAM interface until a processor reset occurs. This issue is sensitive to processor VTT and VDDIO voltage settings.

Potential Effect on System

Undefined system behavior that usually results in a system hang due to a triple fault.

Suggested Workaround

None.

Fix Planned

Yes

Documentation Support

The following documents provide additional information regarding the operation of the processor:

- *BIOS and Kernel Developer's Guide (BKDG) for AMD Family 10h Processors*, order# 31116
- *AMD64 Architecture Programmer's Manual Volume 1: Application Programming*, order# 24592
- *AMD64 Architecture Programmer's Manual Volume 2: System Programming*, order# 24593
- *AMD64 Architecture Programmer's Manual Volume 3: General-Purpose and System Instructions*, order# 24594
- *AMD64 Architecture Programmer's Manual Volume 4: 128-Bit Media Instructions*, order# 26568
- *AMD64 Architecture Programmer's Manual Volume 5: 64-Bit Media and x87 Floating-Point Instructions*, order# 26569
- *AMD CPUID Specification*, order# 25481
- *HyperTransport™ I/O Link Specification* (www.hypertransport.org)

See the AMD Web site at *www.amd.com* for the latest updates to documents.